Claims

[c1] What is claimed is:

1.An electrostatic discharge (ESD) protection circuit electrically connected to an input/output (I/O) buffering pad, an internal circuit, a V_{SS} power terminal, and a V_{DD} power terminal, the ESD protection circuit comprising:

a first ESD-detection circuit electrically connected between the I/O buffering pad and the V_{SS} power terminal;

a P-type substrate-triggered silicon controlled rectifier (P-STSCR) comprising a first lateral silicon controlled rectifier (SCR) and a P-type trigger node, an anode and a cathode of the P-STSCR being electrically connected to the I/O buffering pad and the V_{SS} power terminal respectively;

a second ESD-detection circuit electrically connected between the I/O buffering pad and the V_{DD} power terminal; and

an N-type substrate-triggered silicon controlled rectifier (N-STSCR) comprising a second lateral SCR and an N-type trigger node, a cathode and an anode of the N-STSCR being electrically connected to the I/O buffering pad and the V_{DD} power terminal respectively.

[c2] 2.The ESD protection circuit of claim 1 wherein the P-STSCR further comprises:

a P-type substrate;

an N-well in the P-type substrate;

a first N^+ diffusion region and a first P^+ diffusion region in P-type substrate for use as the cathode of the P-STSCR; and

a second N^+ diffusion region and a second P^+ diffusion region in the N-well for use as the anode of the P-STSCR, the second P^+ diffusion region, the N-well, the P-type substrate and the first N^+ diffusion region forming the first lateral SCR.

[c3] 3.The ESD protection circuit of claim 2 wherein when a positive voltage pulse is applied to the I/O buffering pad, the first ESD detection circuit produces a first trigger current flowing into the P-type trigger node of the P-STSCR to trigger the first lateral SCR in the P-STSCR to enter a latch state, the latch state quickly turning on the P-STSCR so that a current incurred from the positive voltage pulse is discharged to the V_{SS} power terminal.

[c4] 4.The ESD protection circuit of claim 1 wherein the N-STSCR in the ESD protection circuit further comprises:

a P-type substrate;

an N-well in the P-type substrate;

a first N^+ diffusion region and a first P^+ diffusion region in P-type substrate for use as the cathode of the N-STSCR; and

a second N^+ diffusion region and a second P^+ diffusion region in the N-well for use as the anode of the N-STSCR, the second P^+ diffusion region, the N-well, the P-type substrate and the first N^+ diffusion region forming the second lateral SCR.

[c5] 5.The ESD protection circuit of claim 4 wherein when a negative voltage pulse is applied to the I/O buffering pad, the second ESD detection circuit produces a second trigger current that flows into the N-type trigger node of the N-STSCR to trigger the second lateral SCR in the N-STSCR to enter a latch state, the latch state quickly turning on the N-STSCR so that current incurred from the negative voltage pulse is discharged to the V_{DD} power terminal.

[c6] 6.The ESD protection circuit of claim 1 wherein the first ESD protection circuit comprises a first resistor, a first capacitor, a zener diode, a diode string or an NMOS.

[c7] 7.The ESD protection circuit of claim 6 wherein the NMOS enhances the first trigger current so as to accelerate the triggering of the P-STSCR.

[c8] 8.The ESD protection circuit of claim 1 wherein the second ESD detection circuit comprises a second resistor, a second capacitor, a zener diode, a diode string or a PMOS.

[c9] 9.The ESD protection circuit of claim 8 wherein the PMOS enhances the second trigger current so as to accelerate the triggering of the N-STSCR.

[c10] 10.The ESD protection circuit of claim 1 wherein the fist ESD detection circuit comprises a third resistor, a third capacitor and a first inverter, an input node of the first inverter electrically connected to the V_{DD} power terminal and the V_{SS} power terminal through the third resistor and the third capacitor respectively, an output node of the first inverter electrically connected to the P-type trigger node of

the P-STSCR.

[c11] 11.The ESD protection circuit of claim 10 wherein when a positive ESD voltage pulse is applied to the I/O buffering pad, the first inverter is charged by the positive ESD voltage pulse to generate a third trigger current at the output node of the first inverter, the third trigger current flowing into the P-type trigger node of the P-STSCR to trigger the fist lateral SCR, the first lateral SCR entering a latch state in response to the third trigger current and quickly turning on the P-STSCR so that current incurred from the positive voltage pulse is discharged to the V_{SS} power terminal.

[c12] 12.The ESD protection circuit of claim 1 wherein the second ESD detection circuit comprises a fourth resistor, a fourth capacitor, and a second inverter, an input node of the second inverter electrically connected to the V_{SS} power terminal and the V_{DD} power terminal through the fourth resistor and the fourth capacitor respectively, an output node of the second inverter electrically connected to the N-type trigger node of the N-STSCR.

[c13] 13.The ESD protection circuit of claim 12 wherein when a negative ESD voltage pulse is applied to the I/O buffering pad, the output node of the second inverter is charged by the negative ESD voltage pulse to generate a fourth trigger current at the N-type trigger node of the N-STSCR to trigger the second lateral SCR, the second lateral SCR entering a latch state in response to the fourth trigger current to turn on the N-STSCR quickly so that current incurred from the negative voltage pulse is discharged to the V_{DD} power terminal.

[c14] 14.An electrostatic discharge (ESD) protection circuit electrically connected to an I/O buffering pad, an internal circuit, a V_{SS} power terminal and a V_{DD} power terminal, the ESD protection circuit comprising:

a first ESD-detection circuit electrically connected between the I/O buffering pad and the V_{SS} power terminal;

a first stacked silicon controlled rectifier (SCR) electrically connected between the V_{SS} power terminal and the I/O buffering pad, the first stacked SCR series connected by a plurality of P-type substrate-triggered silicon controlled rectifiers (P-STSCR), each P-STSCR comprising a first lateral SCR and a P-type trigger node;

a second ESD-detection circuit electrically connected between the I/O buffering pad and the V_{DD} power terminal; and

a second stacked SCR electrically connected between the V_{DD} power terminal and the I/O buffering pad, the second stacked SCR series connected by a plurality of N-type substrate-triggered silicon controlled rectifiers (N-STSCR), each N-STSCR comprising a second lateral SCR and an N-type trigger node;

wherein a total holding voltage for the first stacked SCR is greater than a maximum voltage level of a normal signal on the I/O buffering pad, and a total holding voltage for the second stacked SCR is less than a minimum voltage level of the normal signal on the I/O buffering pad, so as to prevent normal signals from being interfered because of the unexpected turn-on of the ESD protection circuit by noise.

[c15] 15.The ESD protection circuit of claim 14 wherein each P-STSCR further comprises:

a P-type substrate;

an N-well in the P-type substrate;

a first N^+ diffusion region and a first P^+ diffusion region in the P-type substrate for use as the cathode of the P-STSCR; and

a second N^+ diffusion region and a second P^+ diffusion region in the N-well for use as the anode of the P-STSCR, the second P^+ diffusion region, the N-well, the P-type substrate and the first N^+ diffusion region forming the first lateral SCR.

[c16] 16.The ESD protection circuit of claim 14 wherein the first stacked SCR further comprises a plurality of diodes series connected with each P-STSCR.

[c17] 17.The ESD protection circuit of claim 14 wherein each N-STSCR further comprises:

a P-type substrate;

an N-well in the P-type substrate;

a first N^+ diffusion region and a first P^+ diffusion region in the P-type substrate for use as the cathode of the N-STSCR; and

a second N^+ diffusion region and a second P^+ diffusion region in the N-well for use as the anode of the N-STSCR, the second P^+ diffusion region, the N-well, the P-type substrate and the first N^+ diffusion region forming the second lateral SCR.

[c18] 18.The ESD protection circuit of claim 14 wherein the second stacked SCR further

comprises a plurality of diodes series connected with each N-STSCR.

[c19] 19.A power-rail electrostatic discharge (ESD) clamp circuit electrically connected between a V_{SS} power terminal and a V_{DD} power terminal, the power-rail ESD clamp circuit comprising:
an ESD-detection circuit electrically connected between the V_{SS} power terminal and the V_{DD} power terminal;
at least one substrate-triggered silicon controlled rectifier (STSCR), the STSCR comprising a lateral silicon controlled rectifier (SCR) and at least one trigger node, an anode and a cathode of the STSCR electrically connected to the V_{DD} power terminal and the V_{SS} power terminal.

[c20] 20. The power-rail ESD clamp circuit of claim 19 wherein the STSCR is a P-type substrate-triggered silicon controlled rectifier (P-STSCR) and the trigger node is a P-type trigger node.

[c21] 21.The power-rail ESD clamp circuit of claim 20 wherein when a positive ESD voltage pulse is applied across the V_{DD} power terminal and the V_{SS} power terminal, the ESD detection circuit generates a trigger current that flows into the P-type trigger node of the P-STSCR to trigger the lateral SCR in the P-STSCR so that the lateral SCR enters a latch state and quickly turns on the P-STSCR to discharge current incurred from the positive ESD voltage pulse.

[c22] 22. The power-rail ESD clamp circuit of claim 19 wherein the substrate-triggered silicon controlled rectifier is an N-type substrate-triggered silicon controlled rectifier (N-STSCR) and the trigger node is an N-type trigger node.

[c23] 23.The power-rail ESD clamp circuits of claim 22 wherein when a positive ESD voltage pulse is applied across the V_{DD} power terminal and the V_{SS} power terminal, the ESD detection circuits generates a trigger current to trigger the lateral SCR in the N-STSCR so that the lateral SCR enters a latch state and turns on the N-STSCR to quickly discharge current incurred from the positive ESD voltage pulse.

[c24] 24. The power-rail ESD clamp circuit of claim 19 wherein a plurality of diodes are series connected with the STSCR.

[c25] 25.The ESD protection circuit of claim 19 wherein the substrate-triggered silicon controlled rectifier (STSCR) is a double-triggered silicon controlled rectifier (DT-SCR) and the DT-SCR comprises a P-type trigger node and an N-type trigger node.

[c26] 26.The power-rail ESD clamp circuit of claim 25 wherein the ESD detection circuit comprises:
a resistor electrically connected to the V_{DD} power terminal;
a capacitor electrically connected to the V_{SS} power terminal; and
a first inverter and a second inverter both electrically connected to the V_{DD} power terminal and the V_{SS} power terminal;
wherein when an ESD voltage pulse is applied across the V_{DD} power terminal and the V_{SS} power terminal, the resistor and the capacitor couple a first voltage to an input node of the first inverter so that a second voltage is output from an output node of the first inverter to the P-type trigger node of the DT-SCR and an input node of the second inverter, and causes a third voltage to be output from the output node of the second inverter to the N-type trigger node of the DT-SCR.

[c27] 27.The power-rail ESD clamp circuit of claim 25 wherein the ESD detection circuit comprises:
a first electrical device electrically connected to the V_{DD} power terminal;
a second electrical device electrically connected to the V_{SS} power terminal; and
an inverter electrically connected to the V_{DD} power terminal and the V_{SS} power terminal;
wherein when an ESD voltage pulse is applied across the V_{DD} power terminal and the V_{SS} power terminal, the first electrical device and the second electrical device couple a first voltage to the P-type trigger node of the DT-SCR and an input node of the inverter, and causes a second voltage to be output from an output node of the inverter to the N-type trigger node of the DT-SCR.

[c28] 28.The power-rail ESD clamp circuit of claim 27 wherein the first electrical device a zener diode and the second electrical device is a resistor.

[c29] 29.The power-rail ESD clamp circuit of claim 27 wherein the first electrical device a diode string and the second electrical device is a resistor.

[c30] 30.The power-rail ESD clamp circuit of claim 25 wherein the ESD detection circuit comprises:
a first electrical device electrically connected to the V_{DD} power terminal;
a second electrical device electrically connected to the V_{SS} power terminal;
an inverter electrically connected to the V_{DD} power terminal and the V_{SS} power terminal; and
an NMOS transistor electrically connected to the V_{DD} power terminal;
wherein when an ESD voltage pulse is applied across the V_{SS} power terminal and the V_{DD} power terminal, the first electrical device and the second electrical device couple a first voltage to turn on the NMOS transistor so that the NMOS transistor applies a second voltage to the P-type trigger node of the DT-SCR and an input node of the inverter, and causes a third voltage to be output from an output node of the inverter to the N-type trigger node of the DT-SCR.

[c31] 31.The power-rail ESD clamp circuit of claim 30 wherein the first electrical device a capacitor and the second electrical device is a resistor.

[c32] 32.The power-rail ESD clamp circuit of claim 30 wherein the first electrical device a diode string and the second electrical device is a resistor.

[c33] 33.The power-rail ESD clamp circuit of claim 19 wherein an internal circuit is electrically connected between the V_{SS} power terminal and the V_{DD} power terminal.

[c34] 34.A power-rail ESD clamp circuit for use with mixed voltages, the power-rail ESD clamp circuit being electrically connected between a V_{SS} power terminal and a V_{DD} power terminal, the power-rail ESD clamp circuit comprising a plurality of sub power-rail ESD clamp circuits.

[c35] 35.The power-rail ESD clamp circuit of claim 34 wherein each of the sub power-rail ESD clamp circuits further comprises:
an ESD-detection circuit; and
at least one substrate-triggered silicon controlled rectifier (STSCR), the STSCR comprising a lateral silicon controlled rectifier (SCR) and at least one trigger node.

[c36] 36.The power-rail ESD clamp circuit of claim 35 wherein the STSCR is a P-type

substrate-triggered silicon controlled rectifier (P-STSCR) and the trigger node is a P-type trigger node.

[c37] 37.The power-rail ESD clamp circuit of claim 35 wherein the substrate-triggered silicon controlled rectifier is an N-type substrate-triggered silicon controlled rectifier (N-STSCR) and the trigger node is an N-type trigger node.

[c38] 38.The power-rail ESD clamp circuit of claim 35 wherein the substrate-triggered silicon controlled rectifier (STSCR) is a double-triggered silicon controlled rectifier (DT-SCR) and the DT-SCR comprises a P-type trigger node and an N-type trigger node.

[c39] 39.The power-rail ESD clamp circuit of claim 35 wherein a plurality of diodes are series connected with the STSCR.

[c40] 40.The power-rail ESD clamp circuit of claim 34 wherein the V_{DD} power terminal further comprises a first V_{DD} power terminal and a second V_{DD} power terminal, the power-rail ESD clamp circuit comprises a first sub power-rail ESD clamp circuit, a second sub power-rail ESD clamp circuit and a third sub power-rail ESD clamp circuit.

[c41] 41.The power-rail ESD clamp circuit of claim 40 wherein the first sub power-rail ESD clamp circuit is electrically connected between the first V_{DD} power terminal and the V_{SS} power terminal.

[c42] 42.The power-rail ESD clamp circuit of claim 40 wherein the second sub power-rail ESD clamp circuit is electrically connected between the first V_{DD} power terminal and the second V_{DD} power terminal.

[c43] 43.The power-rail ESD clamp circuit of claim 40 wherein the third sub power-rail ESD clamp circuit is electrically connected between the second V_{DD} power terminal and the V_{SS} power terminal.

[c44] 44.An ESD-connection circuit for use in separated power rails, the separated power rails comprising a first V_{SS} power terminal, a first V_{DD} power terminal, a second V_{SS} power terminal, and a second V_{DD} power terminal, a first core circuit connected between the first V_{DD} power terminal and the first V_{SS} power terminal,

a second core circuit connected between the second V_{DD} power terminal and the second V_{SS} power terminal, the ESD-connection circuit comprising:

at least one ESD-detection circuit;

a first sub ESD-connection circuit;

a second sub ESD-connection circuit;

a third sub ESD-connection circuit; and

a fourth sub ESD-connection circuit.

[c45] 45.The ESD-connection circuit of claim 44 wherein each of the sub ESD-connection circuits further comprises at least one substrate-triggered silicon controlled rectifier (STSCR), the STSCR comprising a lateral silicon controlled rectifier (SCR) and at least one trigger node.

[c46] 46.The ESD-connection circuit of claim 45 wherein the STSCR is a P-type substrate-triggered silicon controlled rectifier (P-STSCR) and the trigger node is a P-type trigger node.

[c47] 47.The ESD-connection circuit of claim 45 wherein the substrate-triggered silicon controlled rectifier is an N-type substrate-triggered silicon controlled rectifier (N-STSCR) and the trigger node is an N-type trigger node.

[c48] 48.The ESD-connection circuit of claim 45 wherein the substrate-triggered silicon controlled rectifier (STSCR) is a double-triggered silicon controlled rectifier (DT-SCR) and the DT-SCR comprises a P-type trigger node and an N-type trigger node.

[c49] 49.The ESD-connection circuit of claim 45 wherein a plurality of diodes are series connected with the STSCR.

[c50] 50.The ESD-connection circuit of claim 45 wherein an anode, a cathode and each trigger node of the first sub ESD-connection circuit are electrically connected to first V_{DD} power terminal, the second V_{DD} power terminal, and the ESD detection circuit, respectively.

[c51] 51.The ESD-connection circuit of claim 45 wherein an anode, a cathode and each trigger node of the second sub ESD-connection circuit are electrically connected to the second V_{DD} power terminal, the first V_{DD} power terminal, and the ESD

detection circuit, respectively.

[c52] 52.The ESD-connection circuit of claim 45 wherein an anode, a cathode and each trigger node of the third sub ESD-connection circuit are electrically connected to the second V_{SS} power terminal, the first V_{SS} power terminal, and the ESD detection circuit, respectively.

[c53] 53.The ESD-connection circuit of claim 45 wherein an anode, a cathode and each trigger node of the fourth sub ESD-connection circuit are electrically connected to the first V_{SS} power terminal, the second V_{SS} power terminal, and the ESD detection circuit, respectively.

[c54] 54.The ESD-connection circuit of claim 44 wherein the ESD-detection circuit is electrically connected between the first V_{DD} power terminal and the first V_{SS} power terminal.

[c55] 55.The ESD-connection circuit of claim 44 wherein the ESD-detection circuit is electrically connected between the second V_{DD} power terminal and the second V_{SS} power terminal.